

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:)
)
Jean BARBIER, et al.) Group Art Unit: TBD
)
Serial No.: Continuation of 10/086,813) Examiner: TBD
)
Filed: March 23, 2004) Attorney Docket No. 003921.00190
)
For: RECONFIGURABLE INTEGRATED)
CIRCUIT WITH INTEGRATED)
DEBUGGING FACILITIES AND)
SCALABLE PROGRAMMABLE)
INTERCONNECT)

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to his duty of good faith and candor as set forth in 37 C.F.R. § 1.56(a) Applicant submits herewith the references cited on the attached PTO form 1449. The cited references were previously cited in parent application Serial No. 10/086,813, filed February 28, 2002, allowed. Applicant respectfully requests that the Examiner consider these references in connection with the search of the prior art required by 37 C.F.R. § 1.104.

Applicant does not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed documents as a competent reference against the claims of the present application.

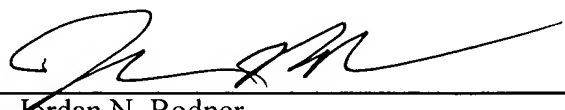
It is respectfully requested that the Examiner fully consider each item of information, initial the enclosed Form PTO-1449 in the appropriate place to indicate that the information has been considered, and return a copy of the initialed form to the undersigned in accordance with MPEP Section 609.

Jean BARBIER, et al.
Attorney Docket No.: 003921.00190

It is believed that no fee is required to ensure consideration of the cited references by the Examiner. However, if a fee is deemed necessary, the Commissioner is authorized to charge our Deposit Account No. 19-0733. A duplicate copy of this sheet is enclosed for accounting purposes.

Respectfully submitted,

BANNER & WITCOFF, LTD.

By: 
Jordan N. Bodner
Registration No. 42,338

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Dated: March 23, 2004

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet 1 of 4

Complete if Known

Application Number	Continuation of 10/086,813
Filing Date	March 23, 2004
First Named Inventor	Jean BARBIER
Art Unit	TBD
Examiner Name	TBD
Attorney Docket Number	003921.00190

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
	1	US- 3,106,698	10/1963	UNGER	
	2	US- 3,287,702	11/1966	BORCK, Jr., et al.	
	3	US- 3,287,703	11/1966	SLOTNIK	
	4	US- 3,473,160	10/1969	WAHLSTROM	
	5	US- 4,020,469	04/1977	MANNING	
	6	US- 4,541,071	09/1985	OHMORI	
	7	US- 4,642,487	02/1987	CARTER	
	8	US- 4,669,061	05/1987	BHAVSAR	
	9	US- 4,700,187	10/1987	FURTEK	
	10	US- 4,706,216	11/1987	CARTER	
	11	US- 4,722,084	01/1988	MORTON	
	12	US- 4,740,919	04/1988	ELMER	
	13	US- 4,758,985	07/1988	CARTER	
	14	US- 4,768,196	08/1988	JOE et al.	
	15	US- 4,786,904	11/1988	GRAHAM	
	16	US- 4,791,602	12/1988	RESNICK	
	17	US- 4,835,705	05/1989	FUJINO et al	
	18	US- 4,849,928	07/1989	HAUCK	
	19	US- 4,870,302	09/1989	FREEMAN	
	20	US- 4,876,466	10/1989	KONDOU et al.	
	21	US - 4,918,440	04/1990	FURTEK	
	22	US- 4,935,734	06/1990	AUSTIN	
	23	US- 4,942,577	07/1990	OZAKI	
	24	US- 4,974,226	11/1990	FUJIMORI et al.	
	25	US- 5,023,775	06/1991	PORET	
	26	US- 5,068,603	11/1991	MAHONEY	
	27	US- 5,084,874	01/1992	WHETSEL, Jr.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				
	28	FRANCE 2 660 510	10/04/1991			
	29					

Examiner
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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Sheet 2 of 4

Complete if Known

Application Number	Continuation of 10/086,813
Filing Date	March 23, 2004
First Named Inventor	Jean BARBIER
Art Unit	TBD
Examiner Name	TBD
Attorney Docket Number	003921.00190

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	30	US- 5,132,974	07/1992	ROSALES	
	31	US- 5,321,828	09/1994	PHILIPS, et al.	
	32	US- 5,425,036	06/1995	LIU, et al.	
	33	US- 5,450,415	09/1995	KAMADA	
	34	US- 5,530,706	06/1996	JOSEPHSON, et al.	
	35	US- 5,553,082	09/1996	CONNOR, et al.	
	36	US- 5,574,388	11/1996	BARBIER, et al.	
	37	US- 5,623,503	04/1997	RUTKOWSKI	
	38	US- 5,680,583	10/1997	KUIJSTEN	
	39	US- 5,777,489	07/1998	BARBIER, et al.	
	40	US- 6,057,706	05/2000	BARBIER, et al.	
	41	US- 3,761,695	09/1973	EICHELBERGER	
	42	US- 4,602,210	07/1986	FASANG	
	43	US- 4,635,261	01/1987	ANDERSON, et al.	
	44	US- 4,758,745	07/1988	ELGAMAL, et al.	
	45	US- 4,855,669	08/1989	MAHONEY	
	46	US- 4,860,290	08/1989	DANIELS	
	47	US- 5,036,473	07/1991	BUTTS	
	48	US- RE. 34,363	08/1993	FREEMAN	
	49	US- 5,329,471	01/1994	SWOBODA	
	50	US- 5,550,843	08/1996	YEE	
	51	US- 4,942,577	07/1990	OZAKI	
	52	US- 4,974,226	11/1990	FUJIMORI, et al.	
	53	US- 4,669,061	05/1987	BHAVSAR	
	54	US- 5,663,813	05/1997	SRINIVASAN	
	55	US- 5,675,589	10/1997	YEE	

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>			Complete if Known		
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			First Named Inventor	Jean BARBIER	
			Group Art Unit	TBD	
			Examiner Name	TBD	
Sheet	3	of	4	Attorney Docket Number	003921.00190

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	56	"The programmable Gate Array Design Handbook, " First Edition, Xilinx, 1986, pp. 1-1 to 4-33.	
	57	Anderson, "Restructurable VLSI Program" Report No. ESD-TR-80-192 (DARPA Contract No. F19628-80-C-002), Mar. 31, 1980.	
	58	Gentile et al., "Design of Switches for Self-Reconfiguring VLSI Array Structures," Microprocessing and Microprogramming, North-Holland, 1984, pp. 99-108.	
	59	Jump, et al., "Microprogrammed Arrays," IEEE Transactions on Computers, vol. C-21, No. 9, Sep. 1972, pp. 974-984.	
	60	Kautz, et al., "Cellular Interconnection Arrays," IEEE Transactions on Computers, vol. C-17, No. 5, May 1968, pp. 443-451.	
	61	Kautz, "Cellular Logic-In-Memory Arrays", IEEE Transactions on Computers, vol. C-18, No. 8, Aug. 1969, pp. 719-727.	
	62	Manning, "An Approach to Highly Integrated, Computer-Maintained Cellular Arrays", IEEE Transactions on Computers, vol. C-26, No. 6, Jun. 1977, pp. 536-552.	
	63	Manning, Automatic Test, Configuration, And Repair of Cellular Arrays, Doctoral Thesis MAC TR-151 (MIT), Jun. 1975.	
	64	Minnick, "Cutpoint Cellular Logic," IEEE Transactions on Electronic Computers, Dec. 1964, pp. 685-698.	
	65	Minnick, "Survey of Microcellular Research," Stanford Research Institute Project 5876 (Contract AF 19(628)-5828), Jul. 1966.	
	66	Pottinger et al., "Using a Reconfigurable Field Programmable Gate Array to Demonstrate Boundary Scan with Built in Self Test," IEEE Computer Society Press, Los Alamitos, CA, US, Proc. Fifth Great Lakes Symposium on VLSI March 16-18 1985, pp. 424-246.	
	67	Sami et al., "Reconfigurable Architectures for VLSI Processing Arrays," AFIPS Conference Proceedings, 1983 National Computer Conference, May 16-19, 1983, pp. 565-577.	
	68	Shoup, "Programmable Cellular Logic Arrays", Doctoral Thesis (Carnegie-Mellon University; DARPA Contract No. F44620-67-C-0058), Mar. 1970.	
	69	Wynn, "Designing With Logic Cell Arrays," ELECTRO/87 and Mini-Micro Northeast Conference Records, 1987.	

Examiner Signature		Date Considered	
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Sheet 4 of 4

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	70	Wynn, "In-Circuit Emulation for ASIC-Based Designs," VLSI Systems Design, Oct. 1986, pp. 38-45.	
	71	Amerson, et al., "PLASMA: An FPGA for Million Gate Systems, FPGA 1996 ACM/SIGDA International Workshop on Field Programmable Gate Arrays.	
	72	Eichelberger & Williams, "A Logic Design Structure for LSI Testability," Design Automation Proceedings, 1977.	
	73	Eichelberger, et al., "Structured Logic Testing," 1991.	
	74	Gokhale, et al. "Splash: A Reconfigurable Linear Logic Array," Jan. 26, 1994.	
	75	Hill, "Preliminary Description of Tabula Rasa, An Electronically Reconfiguration Hardware Engine," 1990 IEEE International Conference on Computer Design: VLSI in Computers & Processors, pp. 391-395.	
	76	Hoflich, "Using the XC4000 Readback Capability," XILINX, XAPP 015.000, pp. 8-37 - 8-44.	
	77	Lee, "On chip Circuitry Reveals System's Logic States," Electronic Design, 1983.	
	78	LSI Logic Chip-Level Full-Scan Design methodology Guide, March 1989.	
	79	PLASMA Chip Specification, August 1, 1995.	
	80	Snider et al., "The Teramac Configurable Compute Engine," Field Programmable Logic and Applications, 5 th International Workshop, FPL '95 Oxford, United Kingdom.	
	81	Sniger, "Teramac Testing: A Quick Sketch," October 1, 1991.	
	82	Williams & Angell, "Enhancing Testability of Large-Scale Integrated Circuits via Test Points and Additional Logic" IEEE Transactions on Computers, January 1973.	
	83		

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